CLAIMS

What is claimed is:

1. A circuit arrangement for interfacing a first circuit arrangement with a bus functioning in accordance with a bus protocol, comprising:

a bus interface circuit having a port arranged to be coupled to the bus, the bus interface circuit providing physical and link layers of the bus protocol;

a bus processing block coupled to the bus interface circuit, the bus processing block implemented with a programmable device and configured to perform selected processing in response to selected bus messages; and

a filter circuit coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with a programmable device and configured to direct bus messages to a selected one of the bus interface circuit and the bus processing block.

2. The circuit arrangement of claim 1, wherein the filter circuit is further configured to direct bus messages to a selected one of the bus interface circuit and the bus processing block in response to at least one of a bus operation code, an address, and initiator identification code in each of the bus messages.

3. The circuit arrangement of claim 1, wherein the filter circuit includes an interior filter circuit coupled to the bus interface circuit and to the bus processing block, the interior filter circuit configured to direct bus messages received from the first circuit arrangement to a selected one of the bus interface circuit and the bus processing block.

4. The circuit arrangement of claim 3, wherein the interior filter circuit is further configured to provide the bus processing block with notification data for selected messages sent to the bus interface circuit.

5. The circuit arrangement of claim 3, wherein the first circuit arrangement includes a cache and a translation look-aside buffer (TLB) that maps virtual addresses to physical addresses of data stored in the cache, the TLB further including a flag with a selected value for selected areas of memory, and the interior filter circuit is coupled to the TLB and further

configured to direct selected bus messages to the bus processing block responsive to the value of the flag in the TLB.

6. The circuit arrangement of claim 3, wherein the first circuit arrangement includes a cache and a translation look-aside buffer (TLB) that maps virtual addresses to physical addresses of data stored in the cache, the TLB further including a flag with a selected value for selected areas of memory, and the interior filter circuit is coupled to the TLB and further configured to provide the bus processing block with notification data for selected messages sent to the bus interface circuit responsive to the value of the flag in the TLB.

7. The circuit arrangement of claim 3, wherein the interior filter circuit includes a ternary content addressable memory (CAM) configured with values representing selected address ranges, and the interior filter circuit is further configured to direct bus messages received from the first circuit arrangement to a selected one of the bus interface circuit and the bus processing block responsive to addresses in the bus messages matching address ranges in the CAM.

8 The circuit arrangement of claim 3, wherein the interior filter circuit includes a ternary content addressable memory (CAM) configured with values representing selected bus message types, and the interior filter circuit is further configured to direct bus messages received from the first circuit arrangement to a selected one of the bus interface circuit and the bus processing block responsive to message types of the bus messages matching values in the CAM.

9 The circuit arrangement of claim 3, wherein the interior filter circuit includes a ternary content addressable memory (CAM) configured with values representing selected address ranges and bus message types, and the interior filter circuit is further configured to direct bus messages received from the first circuit arrangement to a selected one of the bus interface circuit and the bus processing block responsive to addresses and message types of the bus messages matching address ranges and values in the CAM.

10. The circuit arrangement of claim 3, wherein the filter circuit includes an exterior filter circuit coupled to the bus interface circuit and to the bus processing block, the exterior

filter circuit configured to direct bus messages received from the bus to a selected one of the bus interface circuit and the bus processing block.

11. The circuit arrangement of claim 1, wherein the filter circuit includes an exterior filter circuit coupled to the bus interface circuit and to the bus processing block, the exterior filter circuit configured to direct bus messages received from the bus to a selected one of the bus interface circuit and the bus processing block.

12. The circuit arrangement of claim 11, wherein the exterior filter circuit includes a ternary content addressable memory (CAM) configured with values representing selected address ranges, and the exterior filter circuit is further configured to direct bus messages received via the bus to a selected one of the bus interface circuit and the bus processing block responsive to addresses in the bus messages matching address ranges in the CAM.

13. The circuit arrangement of claim 11, wherein the exterior filter circuit includes a ternary content addressable memory (CAM) configured with values representing selected message types, and the exterior filter circuit is further configured to direct bus messages received via the bus to a selected one of the bus interface circuit and the bus processing block responsive to message types of the bus messages matching values in the CAM.

14. The circuit arrangement of claim 11, wherein the exterior filter circuit includes a ternary content addressable memory (CAM) configured with values representing selected address ranges and message types, and the exterior filter circuit is further configured to direct bus messages received via the bus to a selected one of the bus interface circuit and the bus processing block responsive to addresses and message types of the bus messages matching address ranges and message types in the CAM.

15. The circuit arrangement of claim 1, wherein the programmable device is a programmable logic device.

16. The circuit arrangement of claim 1, wherein the programmable device is a field programmable gate array.

17. The circuit arrangement of claim 1, wherein the programmable device is a microcode engine.

18. The circuit arrangement of claim 1, wherein the bus processing block is configured to receive bus messages from the bus without interruption of the first circuit arrangement.

19. The circuit arrangement of claim 1, further comprising a RAM coupled to the bus processing block.

20. The circuit arrangement of claim 1, wherein the bus processing block is configured to initiate transmission of bus messages over the bus via the bus interface circuit.

21. A microprocessor circuit arrangement, comprising:

an instruction execution circuit;

an instruction-fetch circuit coupled to the instruction execution circuit;

a load-store circuit coupled to the instruction execution circuit;

a bus interface circuit coupled to the instruction-fetch circuit and to the load-store circuit and having a port arranged to be coupled to the bus, the bus interface circuit providing physical and link layers of the bus protocol;

a bus processing block coupled to the bus interface circuit, the bus processing block implemented with programmable logic and configured to perform selected processing in response to selected bus messages; and

a filter circuit coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with programmable logic and configured to direct bus messages to a selected one of the bus interface circuit and the bus processing block.

22. The circuit arrangement of claim 21, further comprising:

a memory coupled to the bus processing block;

a cache circuit arrangement coupled to the instruction-fetch and load-store circuits and to the bus processing block, the cache implementing one or more cache layers; and

a translation look-aside buffer (TLB) coupled to the cache and to the bus processing block, wherein the bus processing block is further configured to implement in the memory a cache layer in addition to the one or more cache layers of the cache circuit arrangement.

23. A method for interfacing a first circuit with a bus via an interface arrangement in accordance with a bus protocol, the interface arrangement including a bus interface circuit and a bus processing block, comprising:

receiving at the interface arrangement outgoing bus messages from the first circuit and receiving incoming bus messages from the bus;

selecting a first class of bus messages for processing by the bus processing block and selecting a second class of bus messages for processing by the bus interface circuit;

processing the first class of bus messages at the bus processing block, directing outgoing bus messages in the first class from the bus processing block to the bus interface circuit, and directing incoming bus messages in the first class to the first circuit; and

processing bus messages of the second class at the bus interface circuit in accordance with physical and link layers of the bus protocol.

24. The method of claim 23, wherein the interface arrangement further includes a programmable filter, further comprising configuring the programmable filter for selecting the first and second classes of messages.

25. An apparatus for interfacing a first circuit with a bus via an interface arrangement in accordance with a bus protocol, the interface arrangement including a bus interface circuit and a bus processing block, comprising:

means for receiving at the interface arrangement outgoing bus messages from the first circuit and receiving incoming bus messages from the bus;

means for selecting a first class of bus messages for processing by the bus processing block and selecting a second class of bus messages for processing by the bus interface circuit;

means for processing the first class of bus messages at the bus processing block, directing outgoing bus messages in the first class from the bus processing block to the bus interface circuit, and directing incoming bus messages in the first class to the first circuit; and

means for processing bus messages of the second class at the bus interface circuit in accordance with physical and link layers of the bus protocol.